

ABSTRACT

The present invention facilitates relatively accurate power consumption estimates performed at the register transfer level for scaleable circuits with similar architectural characteristics and features. A power evaluation process of the present invention includes a critical path delay based macro energy model creation process and a scaleable power consumption estimation process. In one embodiment of the present invention, the critical path delay based macro energy model creation process provides a base macro energy table and scaling functions (e.g., a bit width scaling function and a normalizing period scaling function). The scaleable power consumption estimation process utilizes the base macro energy table and scaling functions to estimate power consumption of a circuit. The base energy macro table comprises energy values that are based upon a critical path delay period and correspond to normalized toggle rates . Different bit width circuit toggle rates are converted to normalized toggle rates based upon time periods derived from a normalizing period scaling function. The normalized rates are utilized to lookup an energy per event value that is then scaled in accordance with a bit width scaling function of the present invention. The bit width scaling function is a polynomial function based upon a least square error analysis of sample bit width power consumption values corresponding to average characteristic parameters multiplied by a critical path normalization value (e.g., 1.2 times the critical path delay). The scaled energy per event value is divided by the critical path normalization value to provide an power consumption estimate for a particular bit width.